REMARKS

The following remarks are fully and completely responsive to the Office Action dated October 6, 2004. Claims 1-8 are pending in this application with claims 1-4 and 7 allowed. In the outstanding Office Action, claims 5, 6 and 8 were rejected under 35 U.S.C. § 102(e). No new matter has been added. Claims 5, 6 and 8 are presented for reconsideration.

35 U.S.C. § 102(e)

Claims 5, 6 and 8 were rejected under 35 U.S.C. § 102(e) as being anticipated by Kawamura (U.S. Patent No. 6,670,669 B1). In making this rejection, the Office Action asserts that this reference teaches each and every element of the claimed invention. Applicant requests reconsideration of this rejection.

Claim 5 recites in part:

> a potential switching circuit which supplies a first drain potential to said memory cell transistor at a time of a read operation, and supplies a second drain potential higher than the first drain potential at a time of a write-verify operation.

Claim 8 recites in part:

> a step of reading data from a memory cell transistor at a time of a write-verify operation by applying a second drain potential higher than a first drain potential that is applied to the memory cell transistor at a time of a read operation.

In contrast, Kawamura teaches that the region SD1 serves as both a source and a drain in the read operation described in column 7. Similarly, the region SD2 serves as both a source and a drain in the read operation. This is indicated by the switching of the direction of the current arrows below the transistors shown in Fig. 6 and Fig. 2. Since

the current flows from the source to the drain in each of the read operations described in column 7 and shown in Fig. 6, a voltage of 1.6 V is applied to the source and a voltage of 0 V is applied to the drain.

While Kawamura does not explicitly show the current flow in the transistor for the write-verify operation, one of ordinary skill in the art would expect that the transistor would behave in an identical manner under identical conditions.

Kawamura teaches using the same gate (Vg), SD1, and SD2 voltages in the write-verify operation as used in the read operation. Consequently, the region SD1 also serves as both a source and a drain in the write-verify operation described in column 13. Similarly, the region SD2 serves as both a source and a drain in the write-verify operation.

Therefore, Kawamura teaches applying a source potential of 1.6 V and a drain potential of 0 V at a time of a read operation and applying a source potential of 1.6 V and a drain potential of 0 V at a time of a write-verify operation. Consequently, this reference uses the same drain potential at the time of a read operation and at the time of a write-verify operation.

Therefore, Kawamura fails to teach and/or suggest the claimed invention. Regarding claims 5 and 6, this reference fails to teach and/or suggest "a potential switching circuit which supplies a first drain potential to said memory cell transistor at a time of a read operation, and supplies a second drain potential higher than the first drain potential at a time of a write-verify operation." Regarding claim 8, this reference fails to teach and/or suggest "a step of reading data from a memory cell transistor at a time of a write-verify operation by applying a second drain potential higher than a first drain

potential that is applied to the memory cell transistor at a time of a read operation." Therefore, Applicant requests reconsideration and withdrawal of the rejection of claims 5, 6, and 8 under 35 U.S.C. §102(e).

Conclusion

Applicant's remarks have overcome the objections and rejection set forth in the Office Action dated October 6, 2004. Applicant's remarks have distinguished claims 5, 6 and 8 from Kawamura and thus overcome the rejection of these claims under 35 U.S.C. §102(e). Accordingly, claims 5, 6 and 8 are in condition for allowance. Therefore, Applicant respectfully requests consideration and allowance of claims 5, 6 and 8. Claims 1-4 and 7 are allowed.

Applicant submits that the application is now in condition for allowance. If the Examiner believes the application is not in condition for allowance, Applicant respectfully requests that the Examiner contact the undersigned attorney by telephone if it is believed that such contact will expedite the prosecution of the application.

In the event that this paper is not considered to be timely filed, Applicant hereby petitions for an appropriate extension of time. The Commissioner is authorized to charge payment for any additional fees which may be required with respect to this paper to our Deposit Account No. 01-2300, making reference to attorney docket number 100353-00179.

Respectfully submitted,
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